EE4101E: RF Communications

Low Noise Amplifier Design Using ADS (Report)

SEM 1: 2014/2015

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INTRODUCTION

The project is based on the design simulation of low noise amplifier using advance design software ADS. The design methodology required the design of proper DC biasing network, the analysis of the transistor stability, input and output matching network selection etc. The design for low noise amplifier with below specifications, a single stage LNA amplifier with NE3210S01 at 4.4 GHz is used for our project.

Amplifier Specification

Center Frequency	**4.4GHz**
Noise Figure	**<1dB**
Gain	**As High As Possible**
Source Impedance	**50 Ohms**
Load Impedance	**50 Ohms**
Relative Permittivity of Substrate	**2.20**
Thickness of Substrate	**1.6 mm**
Transistor	**NEC NE3210S01 HJ-FET**

OBJECTIVE

Main objective of this project is to learn basics of ADS and also learn how to design a low noise amplifier for a desired frequency. The low noise amplifier is a spcial type of electronic amplifier used in communication systems, which amplifies very weak signals captured by an antenna. This is frequently used in microwave system like GPS. Advanced Design System (ADS) is the world's leading electronic design automation software for RF, microwave, and high-speed digital application.

SPECIFICATION OF NE3210S01

NEC's NE3210S01 is a pseudomorphic Hetero-Junction FET that uses the junction between Si-doped AIGaAs and undoped InGaAs to create very high mobility electorns. Its excellent low noise and associated gain make it suitable for DBS and another commercial system. It has Super Low Noise Figure and High Associated Gain for example, NF=0.35dB TYP. Ga=13.5dB TYP at f=12 GHz. However, its stability is below 8GHz is not quite satisfactory.

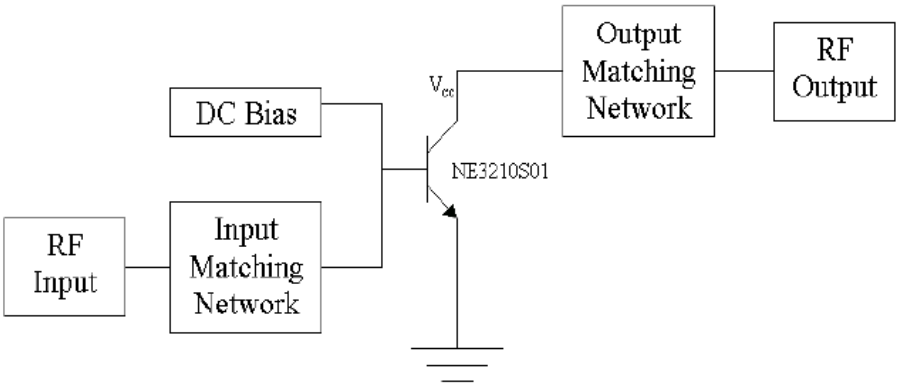


Fig.1.General Circuit Layout

DESIGN METHODOLOGY OF LNA

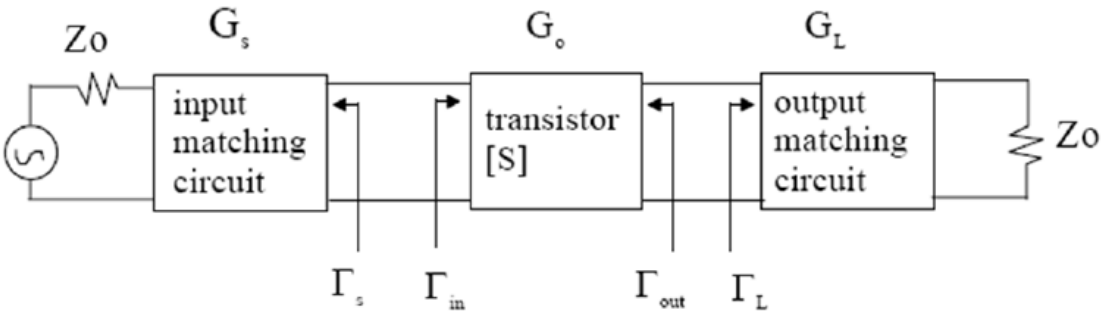


Fig.2. shows a single transistor amplifier with matching networks at the input and output terminals of the transistor.

The following are common design procedure for LNA:

1. Check stability perfomance
2. If the transistor is potentially unstable, it can be stabilized by adding a feedback resistor from drain to the source or a ballast resistor at the drain, but it would increase the noise figure.
3. Choosing between unilateral and bilateral design by calculating unilateral figure.
4. Calculate NFmin, Γ_{opt} of the transistor from the S-parameter.
5. For a unilateral case, the constant gain circles for the desired or maximum gain is used for bilateral case, the available power gain circle for the desired or maximum gain should be used.
6. Choose a Γ_s value which is in the stable region as well as within the noise circle and the corresponding gain circle.

7. Γ_L can be calculated then from values of Γ, the corresponding impedance values Zs and Z can be obtained. Then these impedence values have to be matched with their corresponding Source and load impedence Zo (in most cases 50 ohms).
8. The impedence matching networks (input and output) are designed using the smith chart. This can be achieved using LC based network or distributed elements like open or short circuited stubs combined with a length of transmission line.
9. Provide DC bias for the Q point based on the data sheet.

IMPLEMENTING DESING USING ADS

1. Obtain the FET model of NE3210S01 from the manufacture website as Figure (1).

Then choose the right path name and add ports to the transistors and save the design as NE3210S01 for later design and simulation.

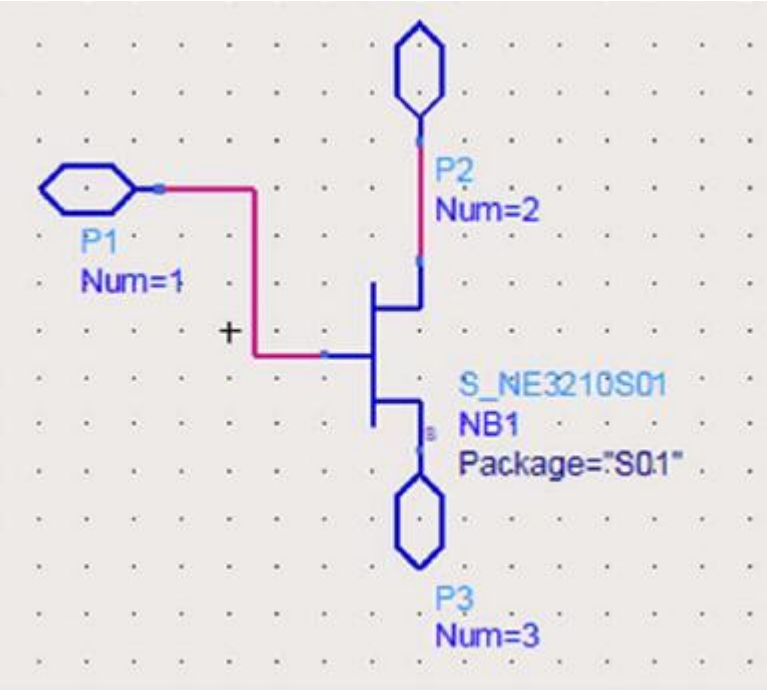


Figure (1)

2. DC Bias Circuit Design

DC tracing

Insert the FET model of NE3210S01 from previous part which is saved in library.

DC tracing parameters are set according to VI curve (Vgs -0.63V to 0V) from NE3210S01 datasheet. Connect D to port2 (Drain), G to port1 (Gate),Port3(Source) to GND, refer to Figure (2).

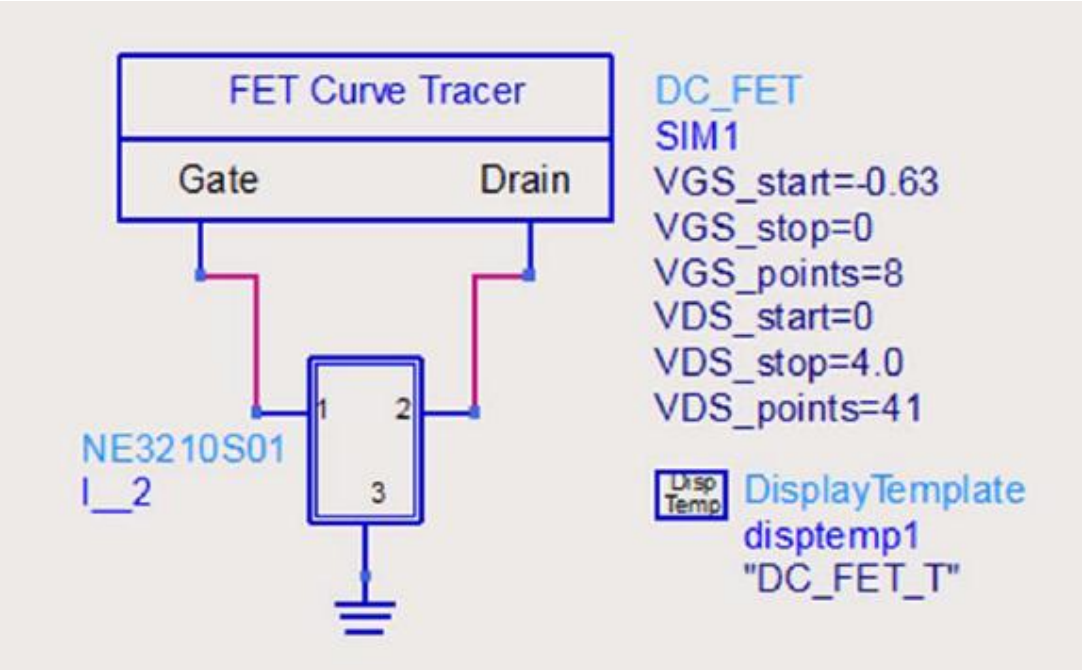


Figure (2)

After simulation, the result has shown in Figure (3).

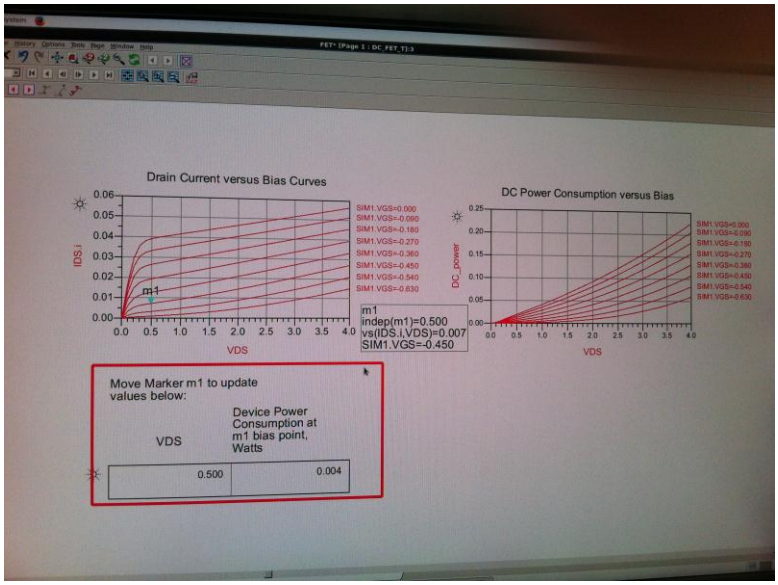


Figure (3)

The operation point is determined from NE3210S01 datasheet.

At 4.4 GHz, the NFmin is about 0.4dB at Vds=2V and Ids=10mA and the gain is about 18dB.

Bias circuit design and verification

To verify the biasing point, DC simulation is used. After simulation, the bias circuit network is shown in the following graph, Figure (4). It can be seen that Vds and Ids are 2V and 10mA as desired.

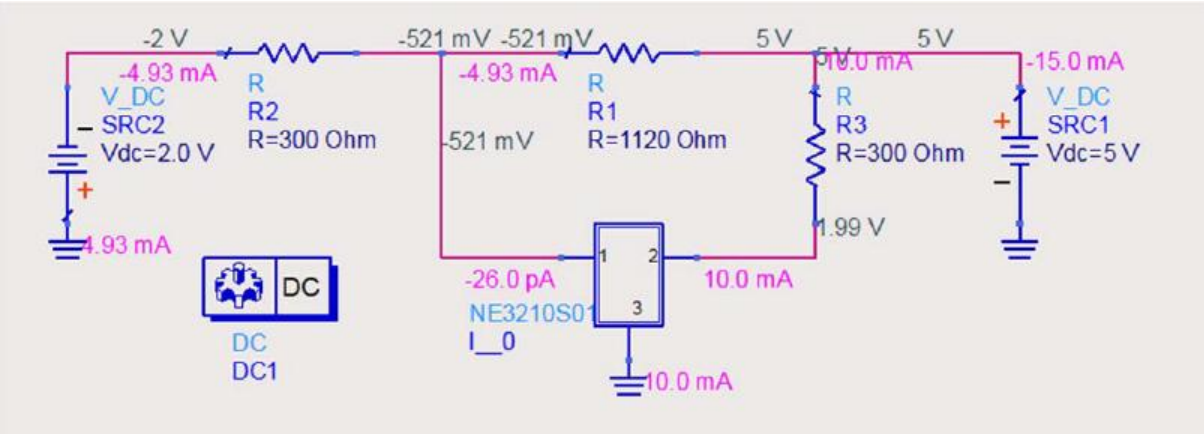


Figure (4)

S-parameters, NF and stability

To determine S-parameters, NF and stability, the schematic is drawn as per Figure (5).

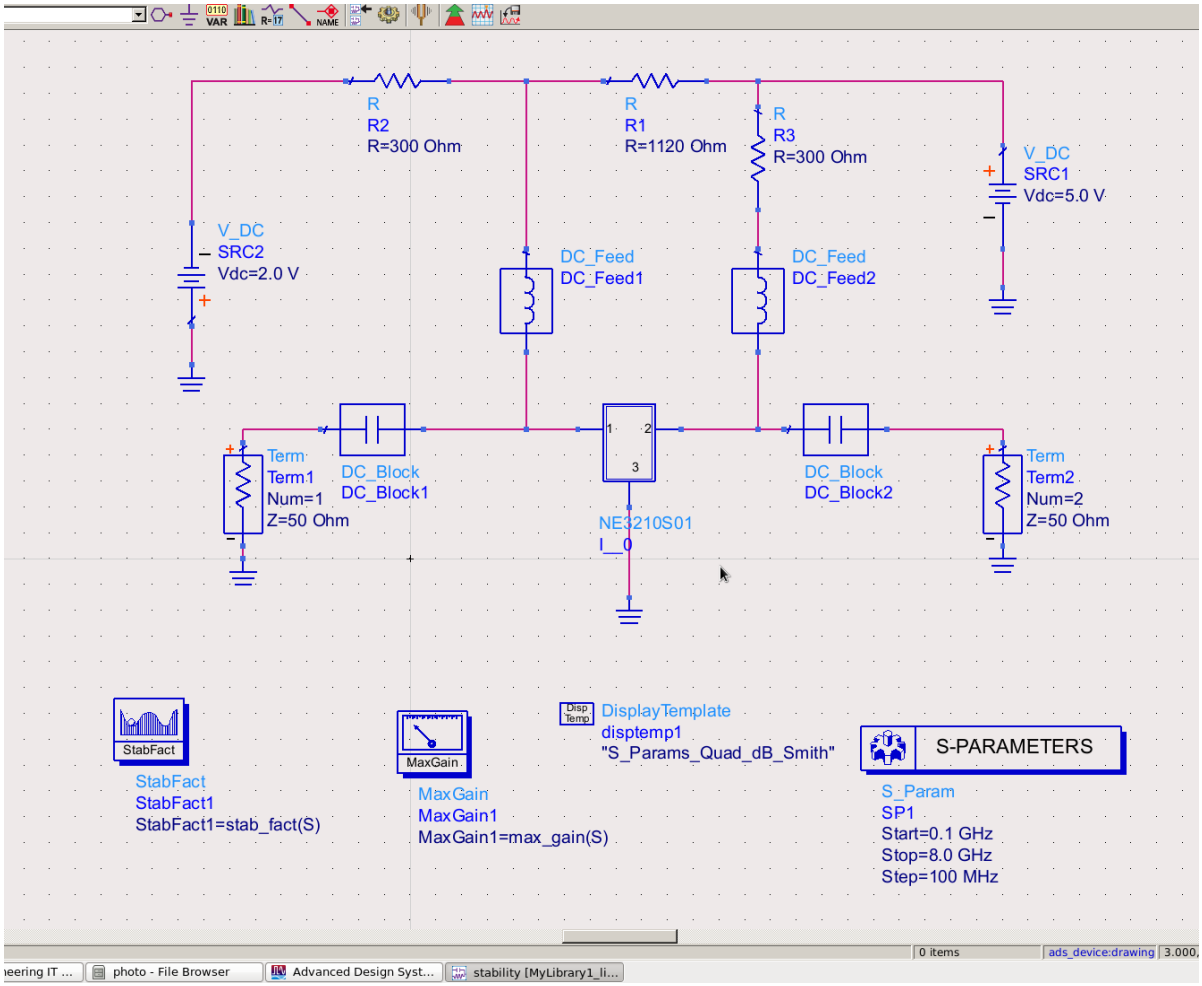


Figure (5)

After simulation of the schematic Figure (5), maximum gain and stability factor is plotted as per Figure (6) to see whether LNA is stable at desired frequency. In Figure (6), it can be seen that the maximum gain is 20.120 and stability factor is 0.450 (less than 1) at 4.4GHz. LNA might be unstable so the LNA need to be stablized.

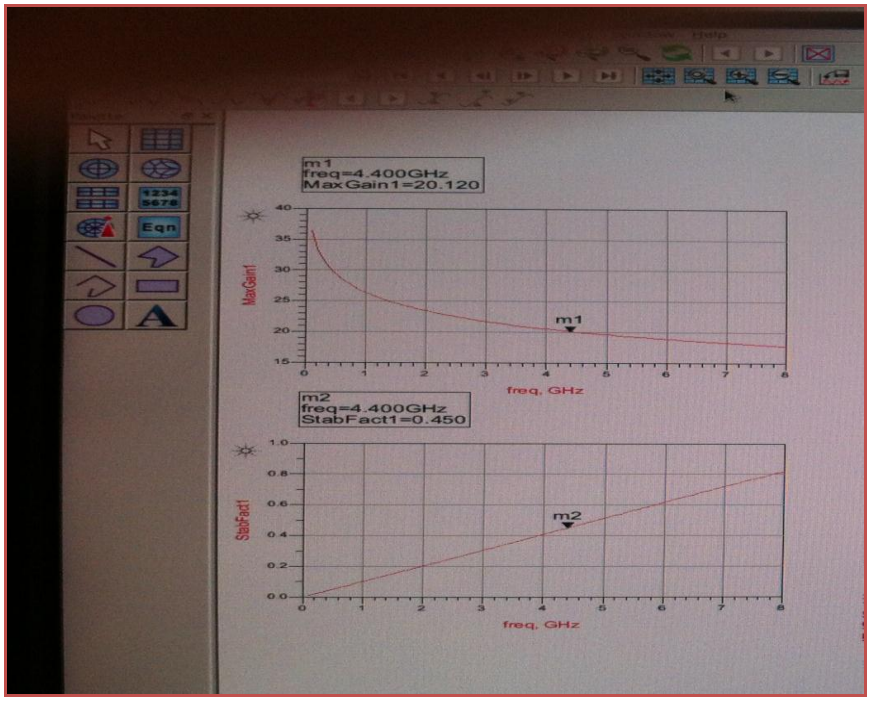


Figure (6)

The most common method to stabilize a system is to use a negative feedback. Two small inductors are added at both sources of the NE3210S01 to create the feedback path as per below Figure(7).

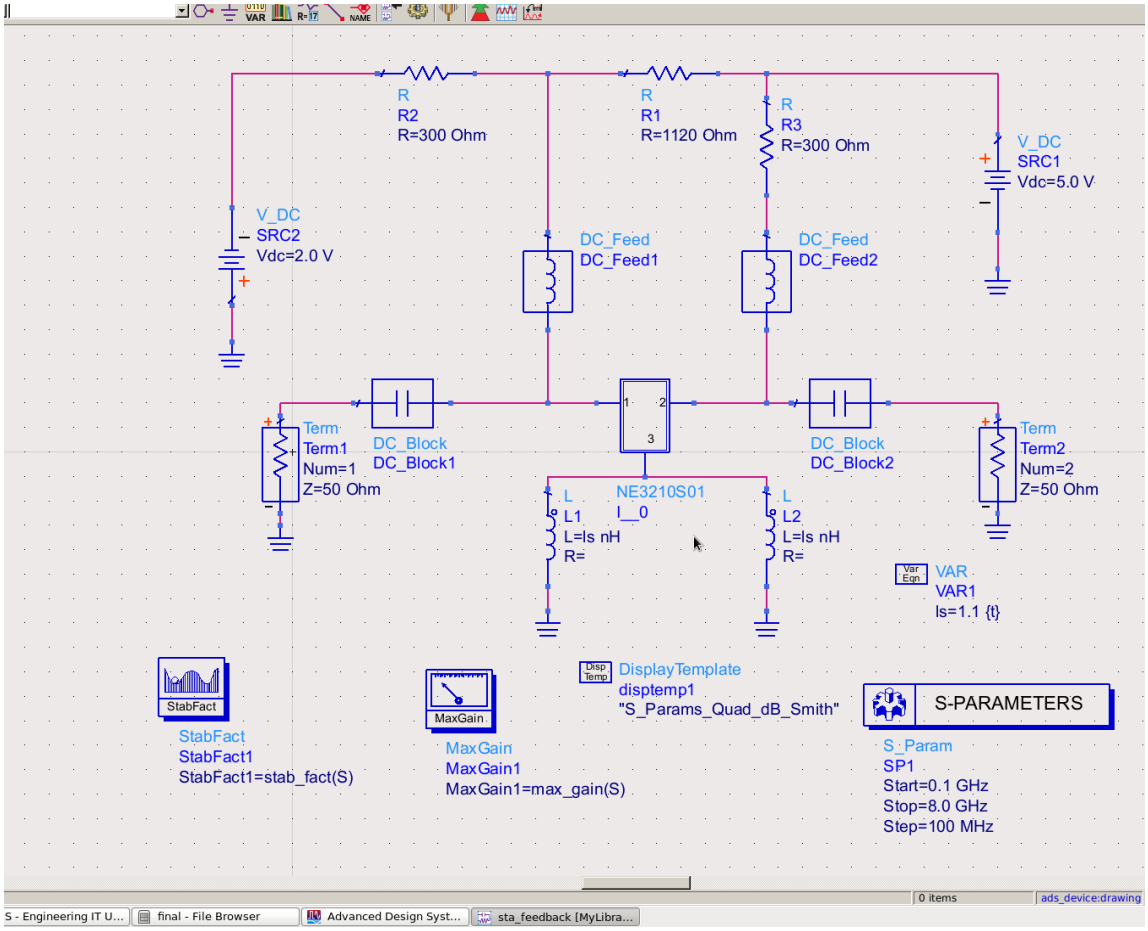
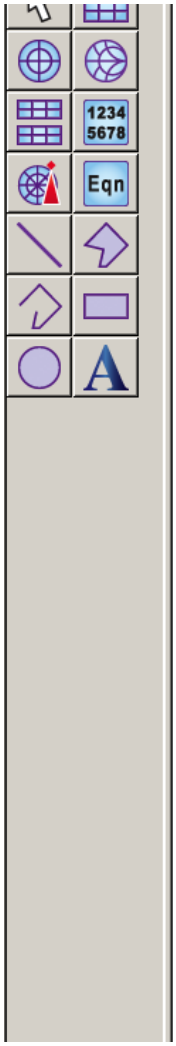


Figure (7)

After simulation of schematic, L is tuned to get optimum value. The optimum L value is achieved as 1.1 as per Figure (7).

The maximum gain reduces from 20dB to 16.389dB as per Figure (8) due to negative feedback. However, there is still stability problem at low frequency.



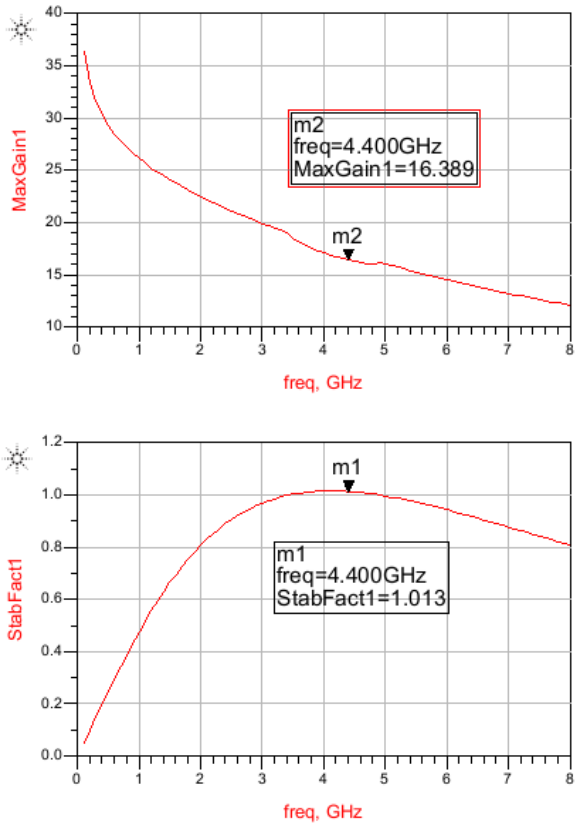


Figure (8)

At low frequency, the stability problem can be remedied by using small value terminating resistors.

Therefore, the DC Feed ideal components are replaced with real inductors as per Figure (9).

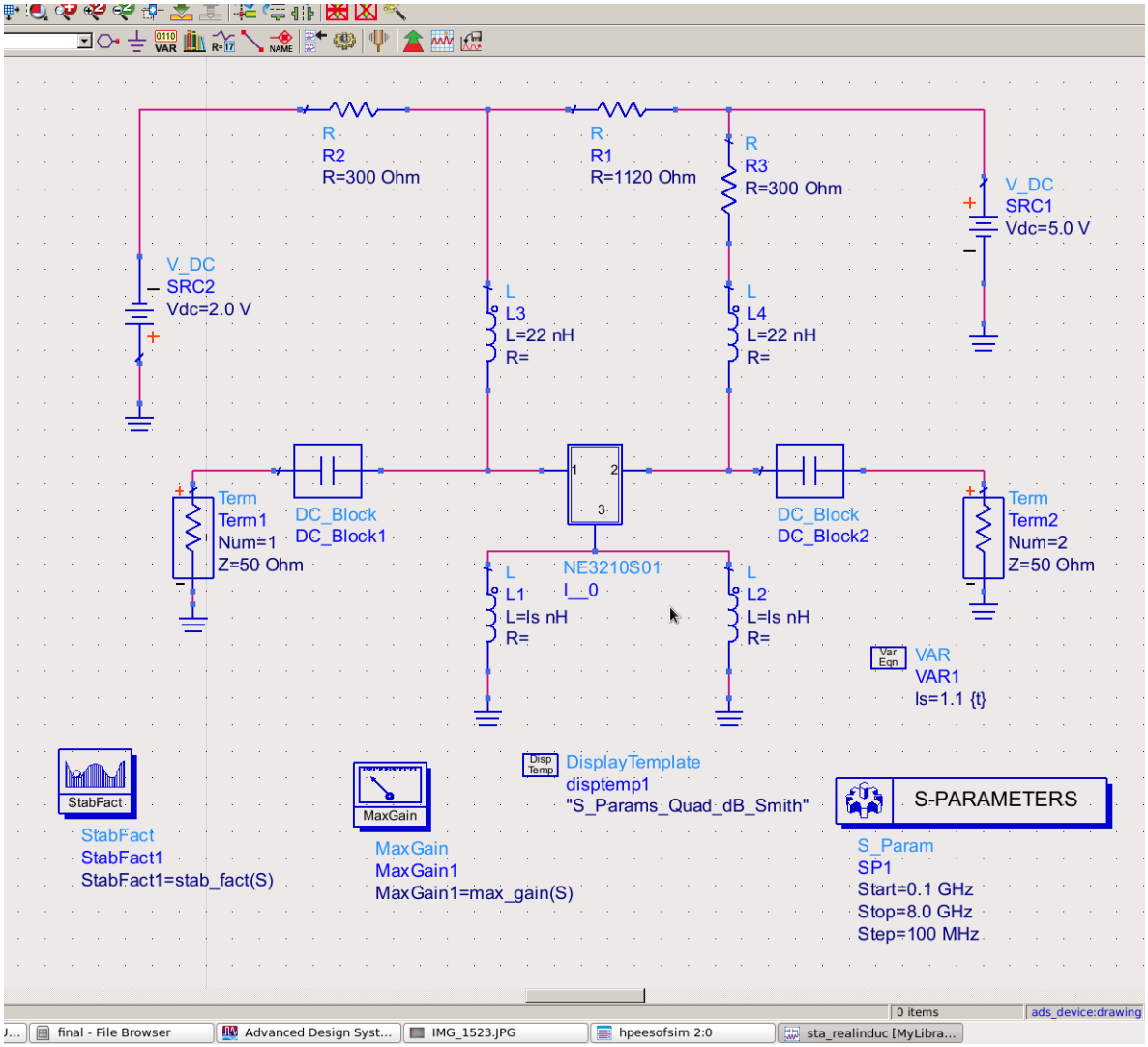


Figure (9)

After simulation, the maximum gain and stability factor are seen as per Figure (10).

The stability factor (1.013 to 1.241) at low frequency is improved quite obviously and the gain reduction (16.389dB to 14.119dB) is observed.

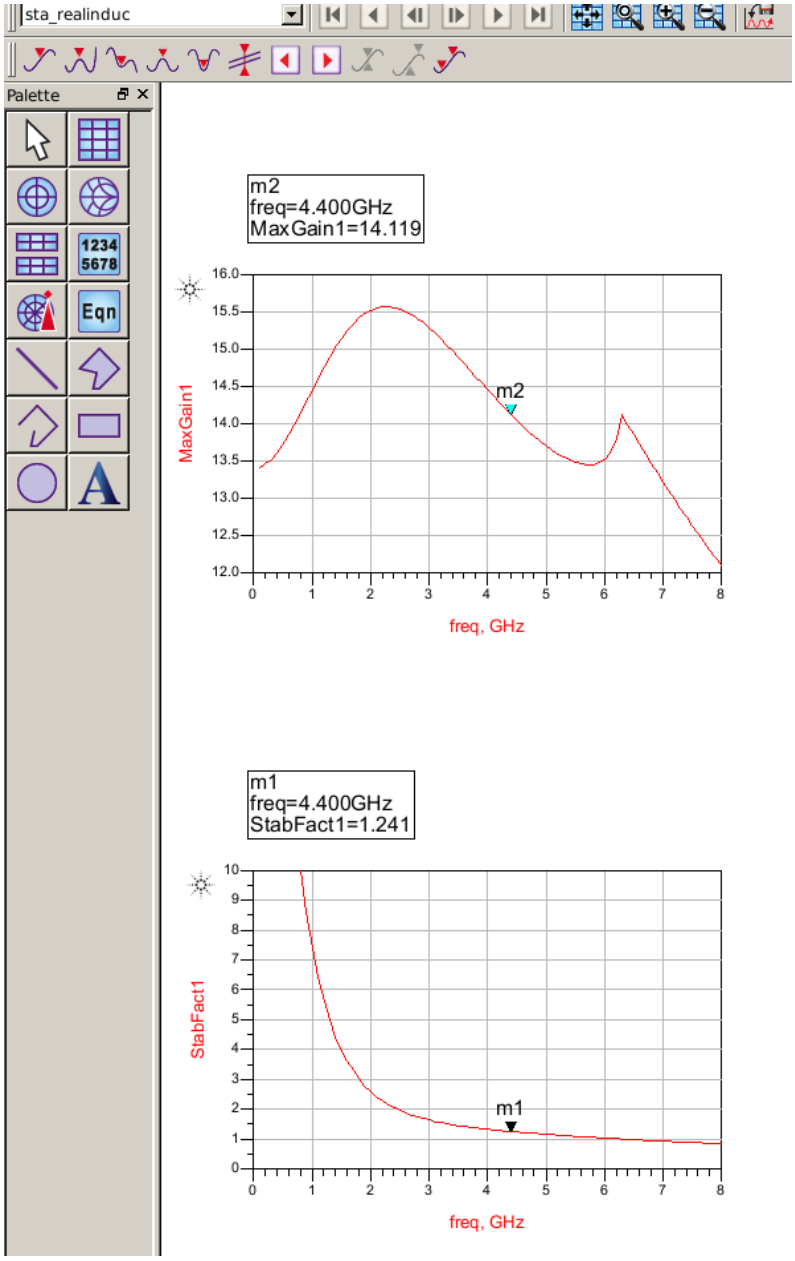


Figure (10)

To achieve better maximum gain and stability factor, a small value inductor can be implemented with a high transmission line. Two transmission lines are inserted with the length of Ls at the source terminals and proper length is determined using simulator as per Figure (11).

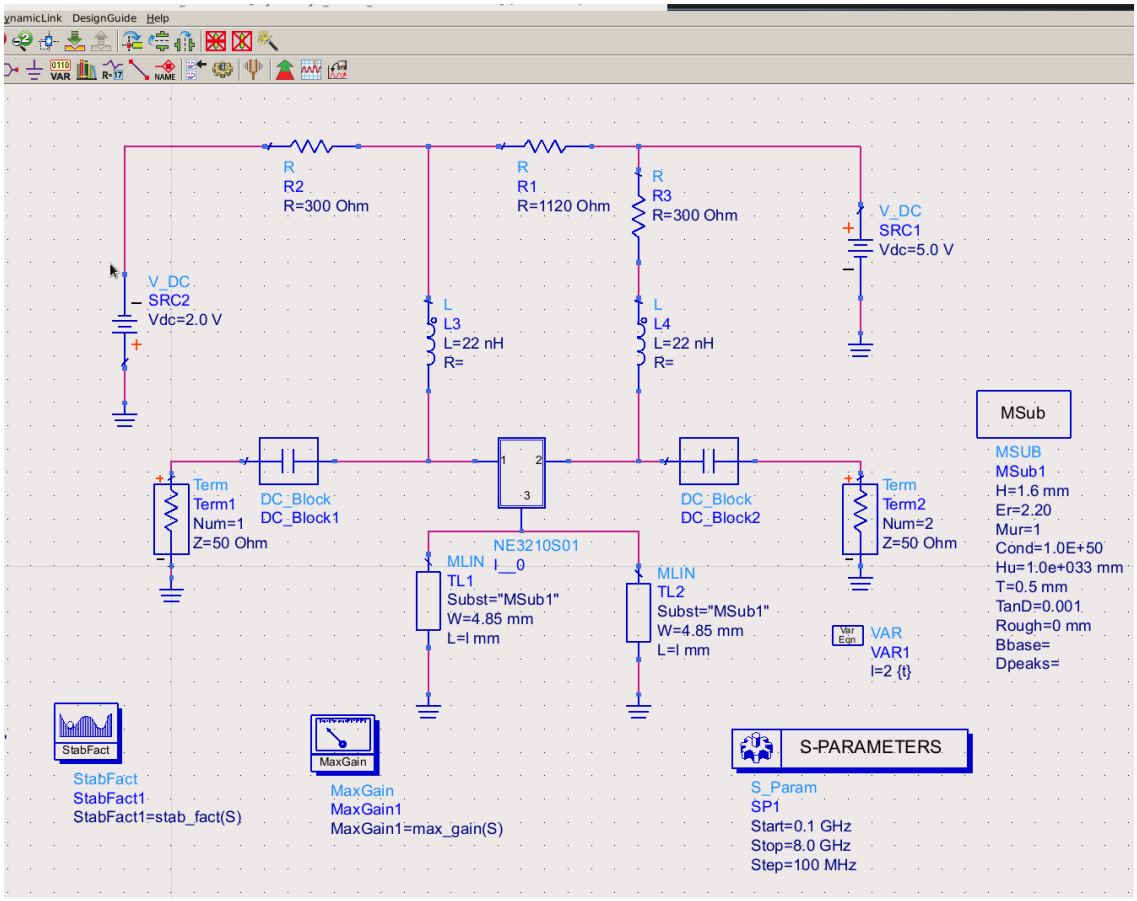


Figure (11)

After simulation Figure (11), the maximum gain and stability factor are achieved as per Figure (12).

Now the stability factor and gain are OK.

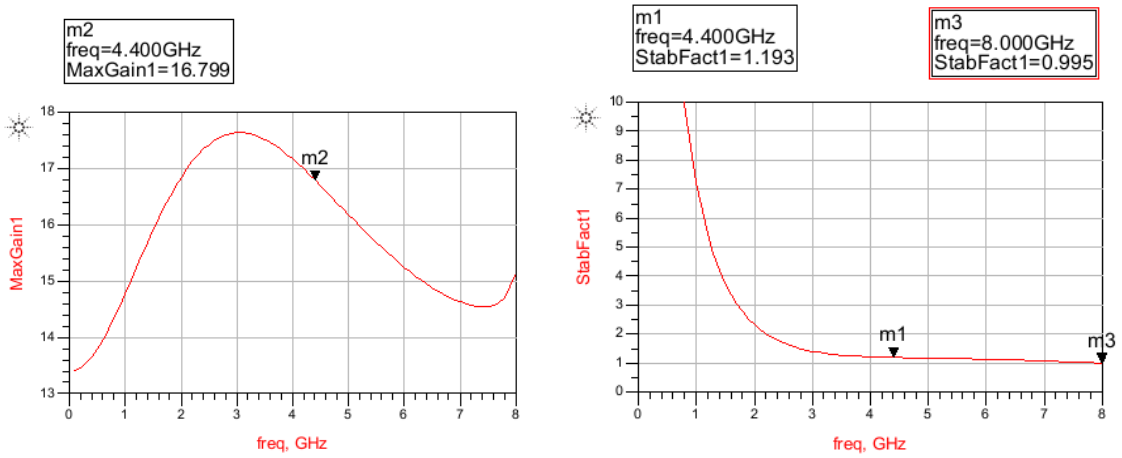


Figure (12)

Ideal DC blocks are replaced with real capacitors as per Figure (13).

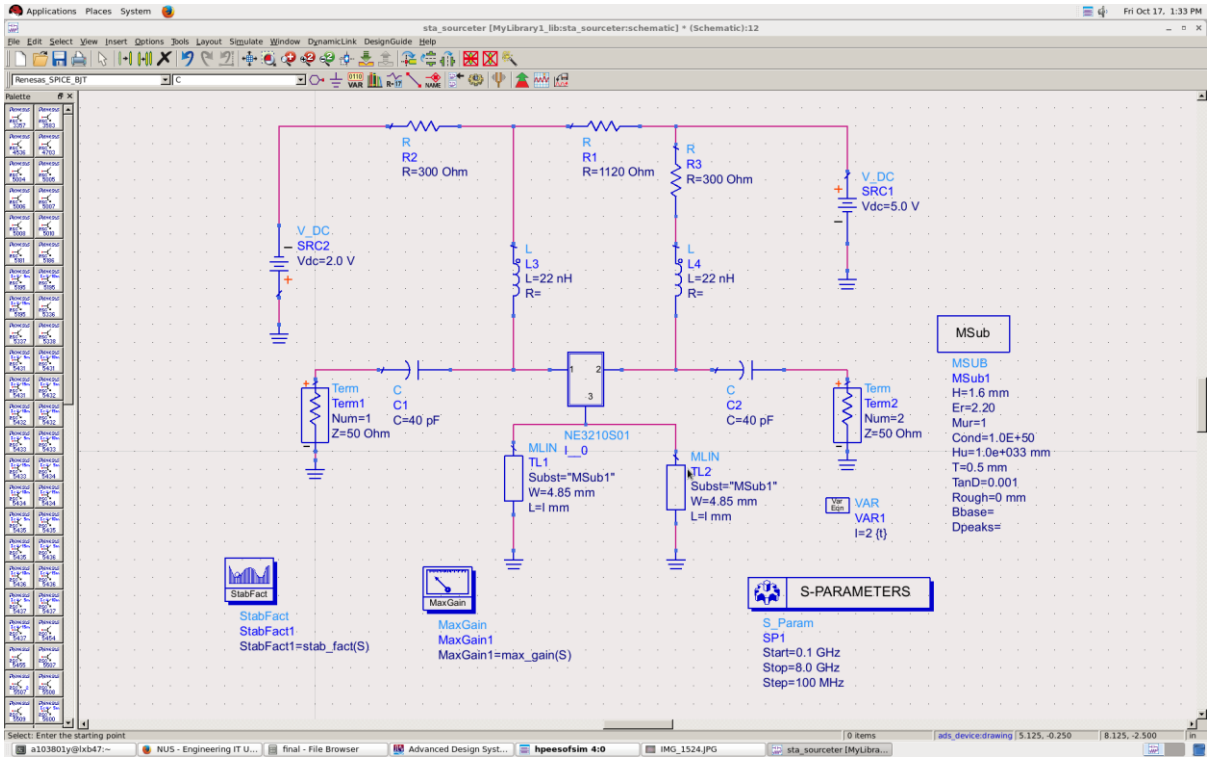


Figure (13)

Noise Circle and input matching

To calculate noise, NF min is plotted as per Figure (14).

It can be seen that the minimum NF is about 0.807dB at 4.4GHz.

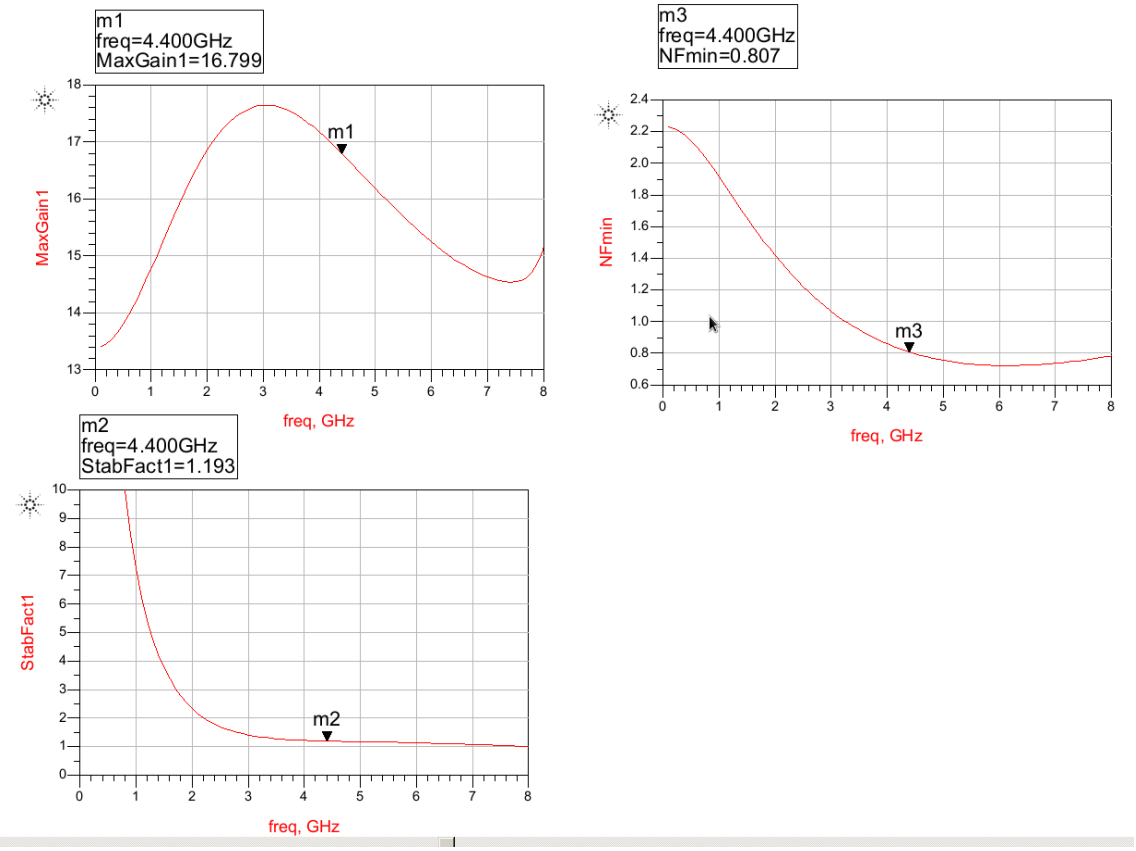


Figure (14)

A proper input matching network is determined to get the minimum NF.

Smith Chart is plotted and GaCircle and circleData are selected from the Equation dataset.

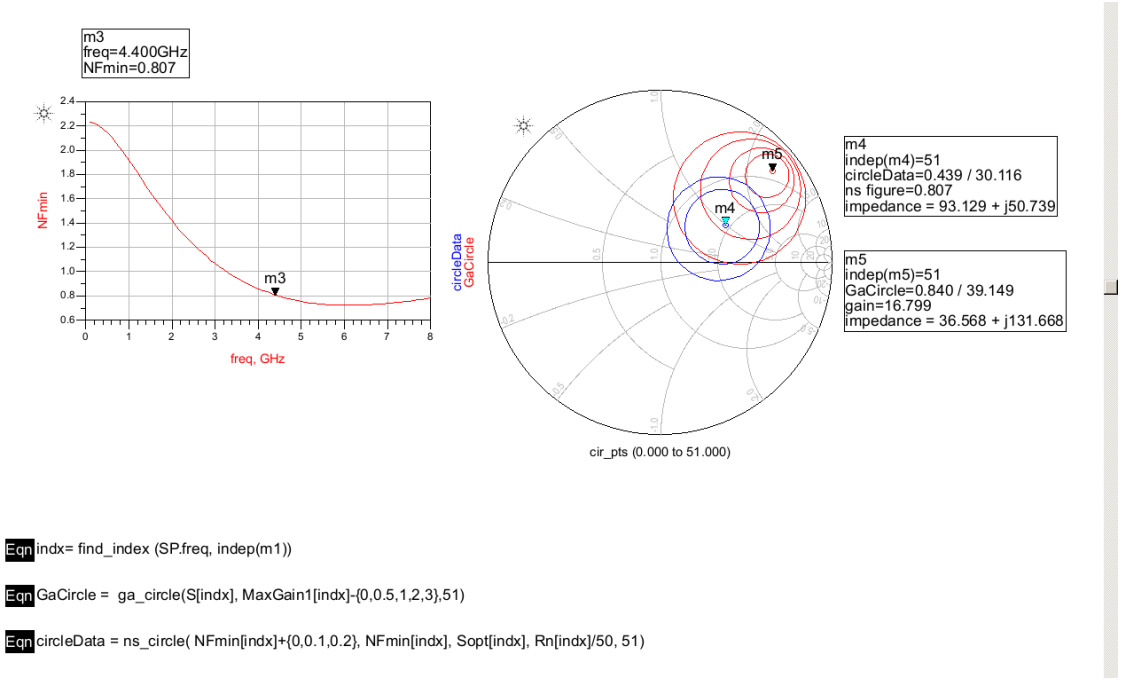


Figure (15)

Initially, it can be seen that the optimum point for Gain(m1) and NF (m3) are located at different location. For the optimum NF, the gain needs to be sacrificed.

At 15.142dB constant gain circle, the optimum NF can be obtained. Hence, the optimum source impedance is 90.226+j48.646.

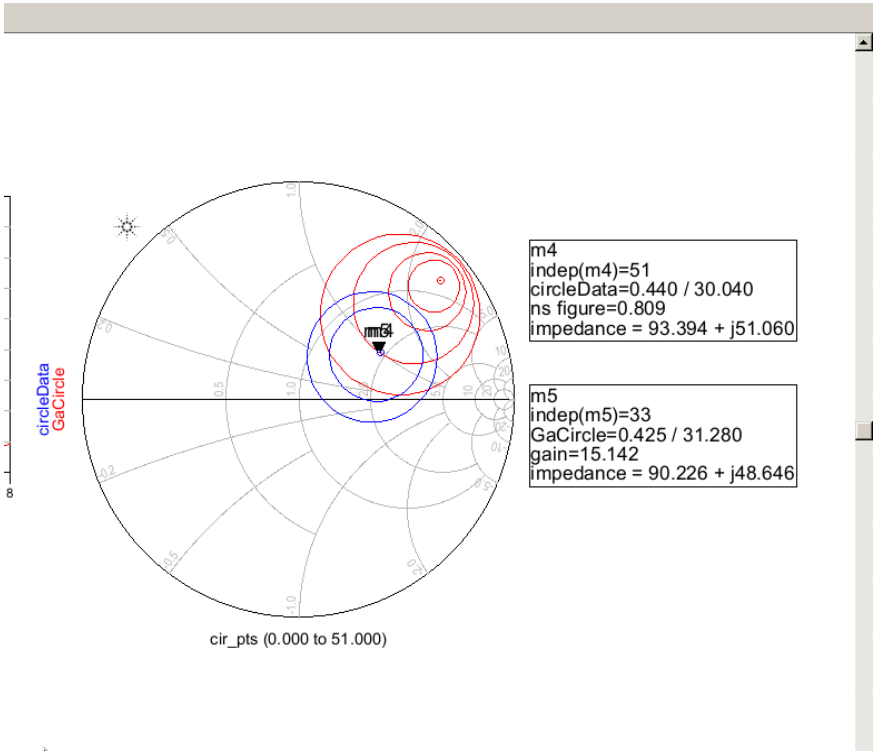


Figure (16)

To design input matching, AD_SmithChartMatch utility is inserted in the ADS as shown in Figure (17).

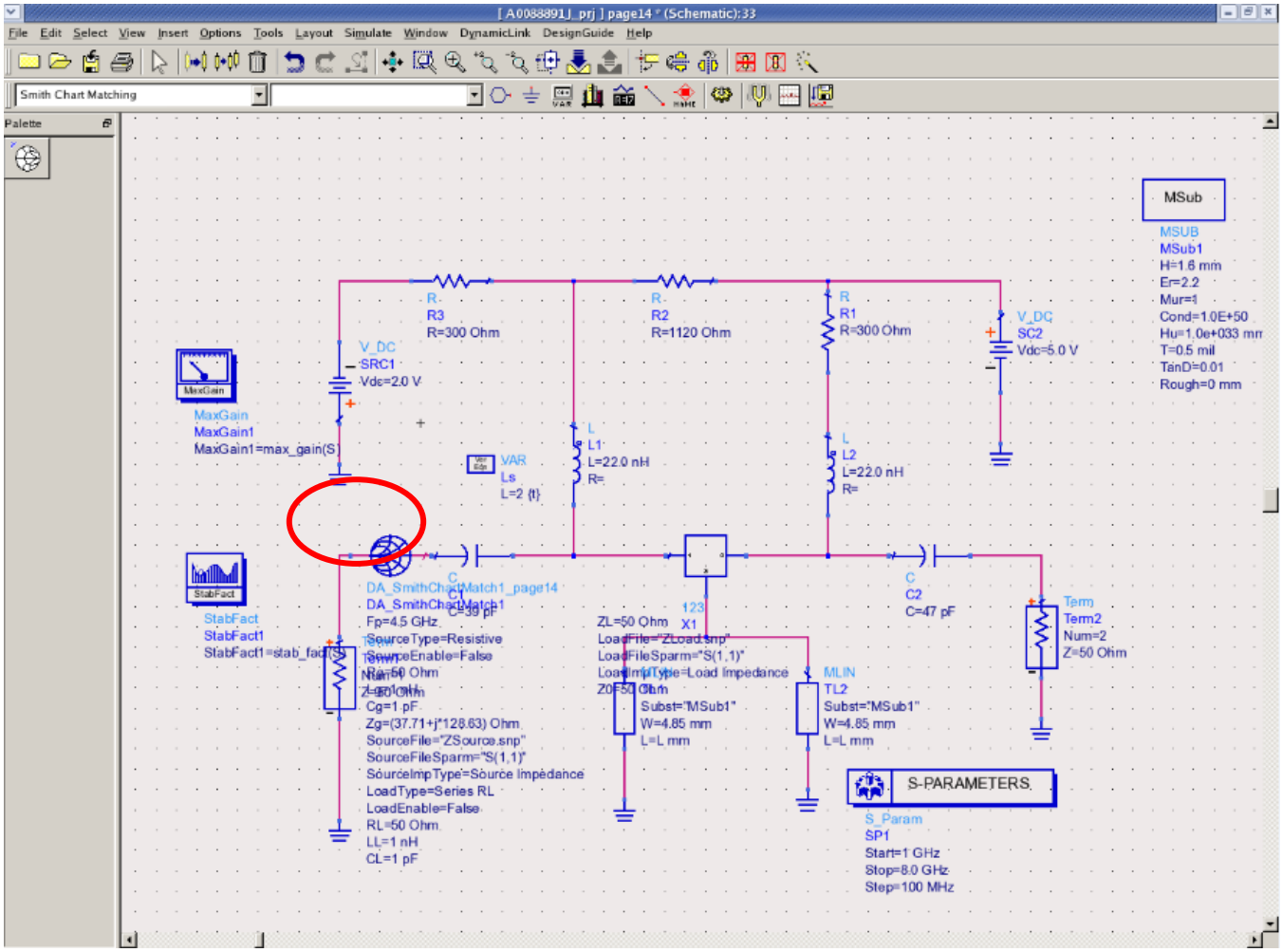


Figure (17)

Under the smith chart utility window shown in Figure (18), we set frequency 4.4 GHz (which is the given frequency for our team to work on). Set the source impedance value as 90.226+j48.646, which we have selected in Figure (16). Then place matching components for shunt and series.

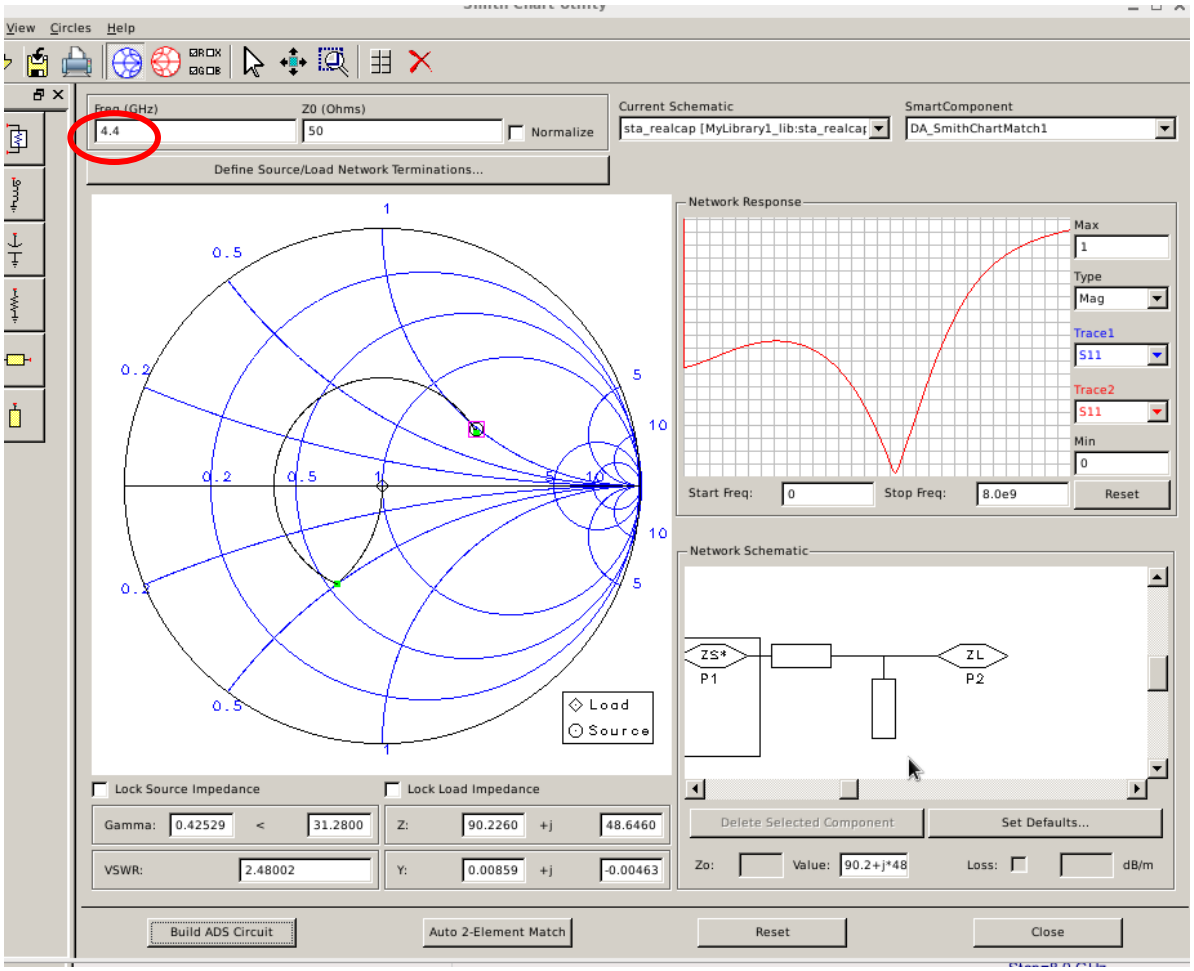


Figure (18)

Simulated result is as shown below in Figure (19).

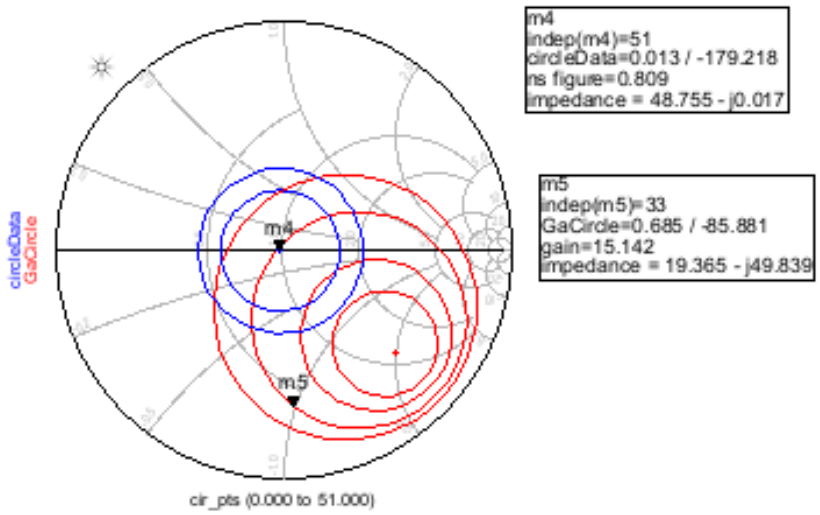


Figure (19)

Coupling capacitor at the input will cause a complication in the circuit construction, therefore we swap the coupling capacitor and the matching network as shown below in Figure (20).

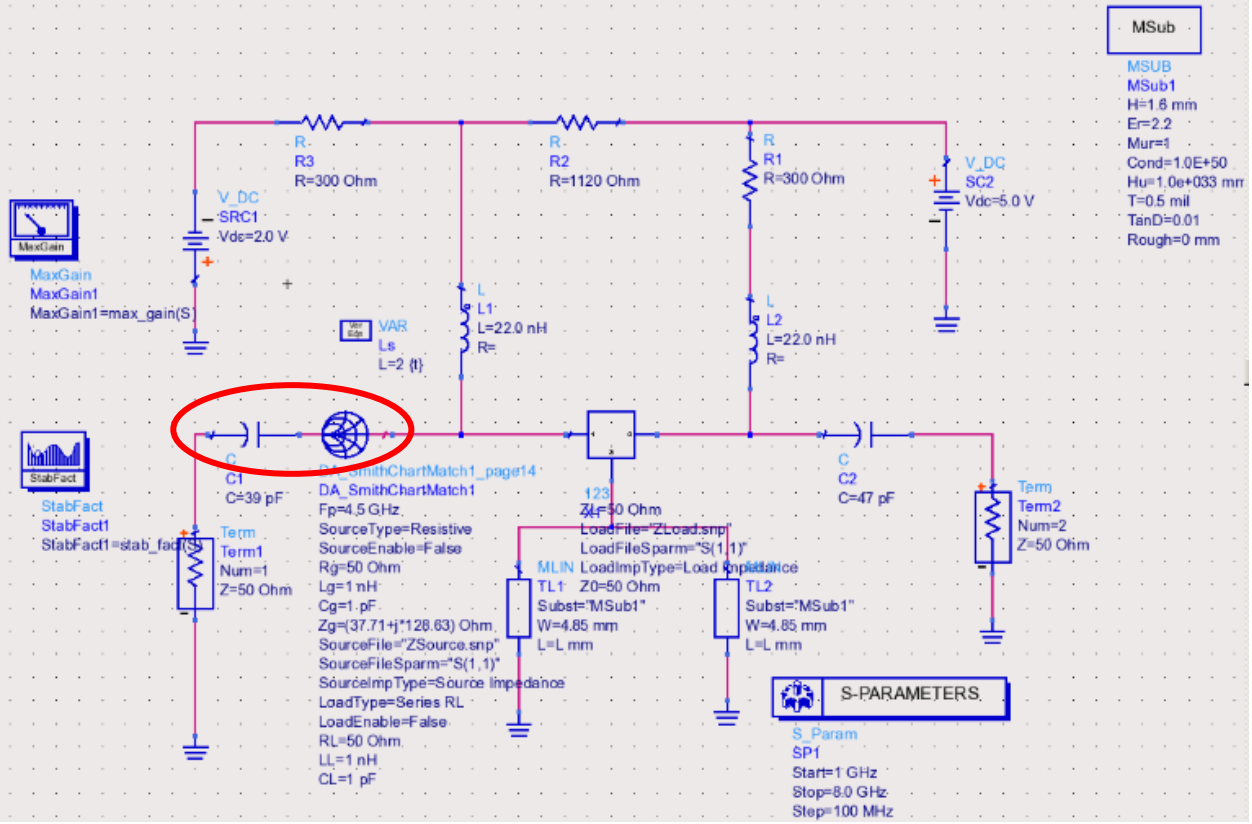


Figure (20)

We replace AD_SmithChartMatch utility with T Lines – Microstrip shunt and series. The updated ADS is shown below in Figure (21).

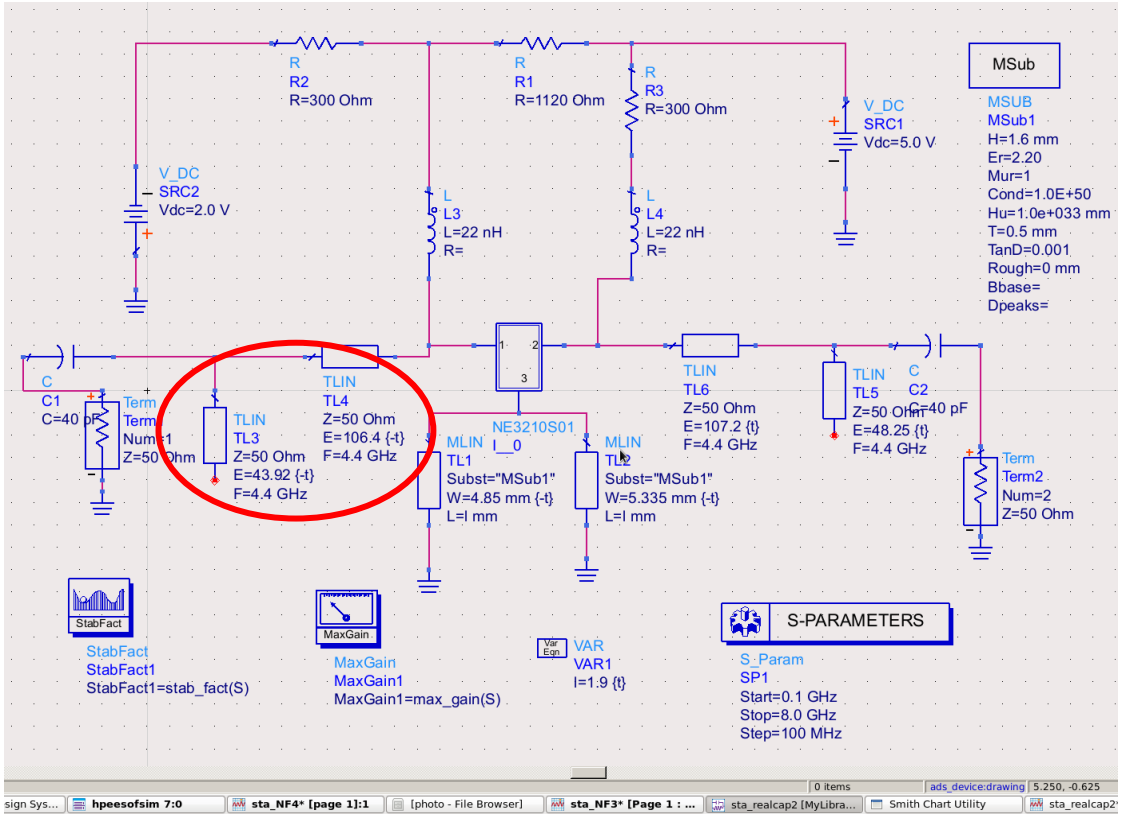
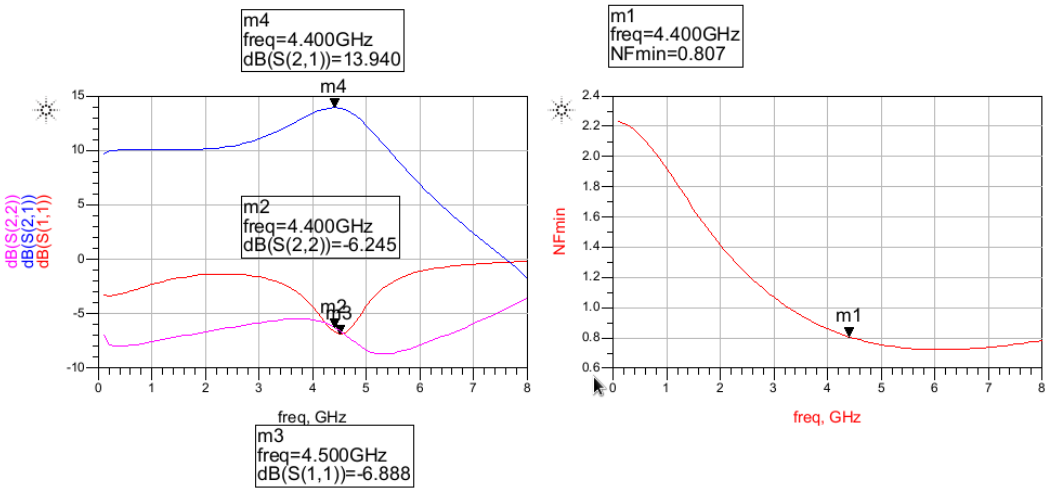


Figure (21)

The result of Gain, Output return loss, output return loss NF and stability factors are shown in Figure (22). It can be seen that gain can be improved by the output matching network. In Low noise amplifier, output matching network will not interfere with noise figure and only input impedance influence noise figure.



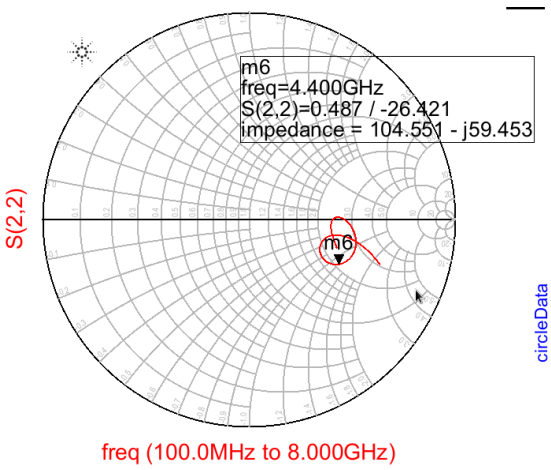


Figure (22)

Output Matching for Gain

To design input matching, AD_SmithChartMatch utility is inserted in the output side as shown in Figure (23).

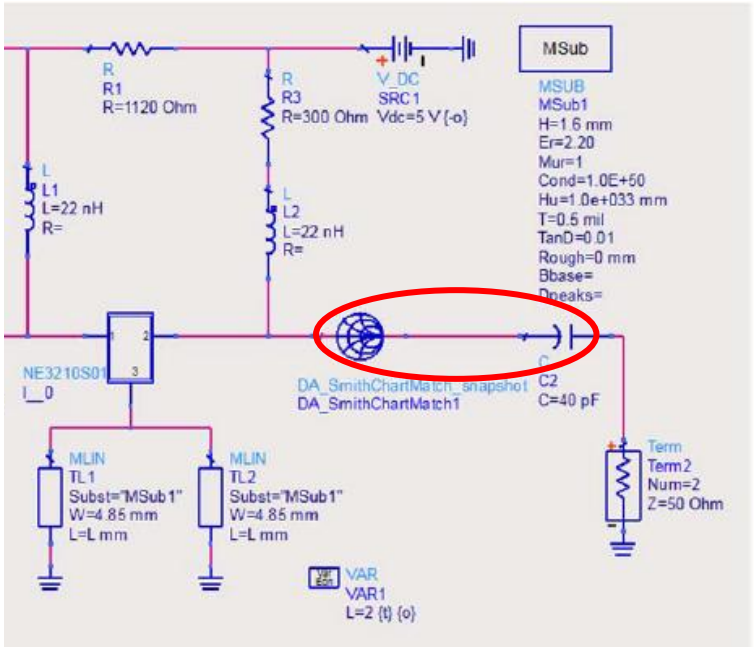


Figure (23)

Under the smith chart utility window shown in Figure (24) for output matching, Set the source impedance value as 104.551-59.453, which we derived from Figure 22. Then place matching components for shunt and series.

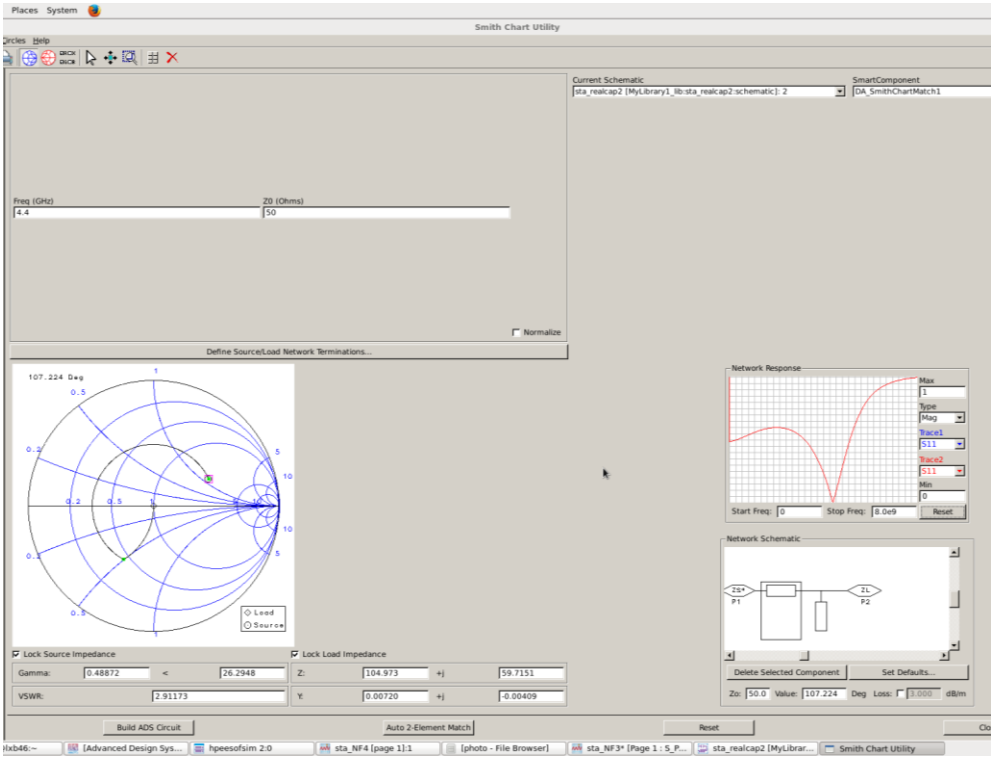


Figure (24)

Once we acquired shunt and series for output matching, we replace them in the ADS as shown below in Figure (25).

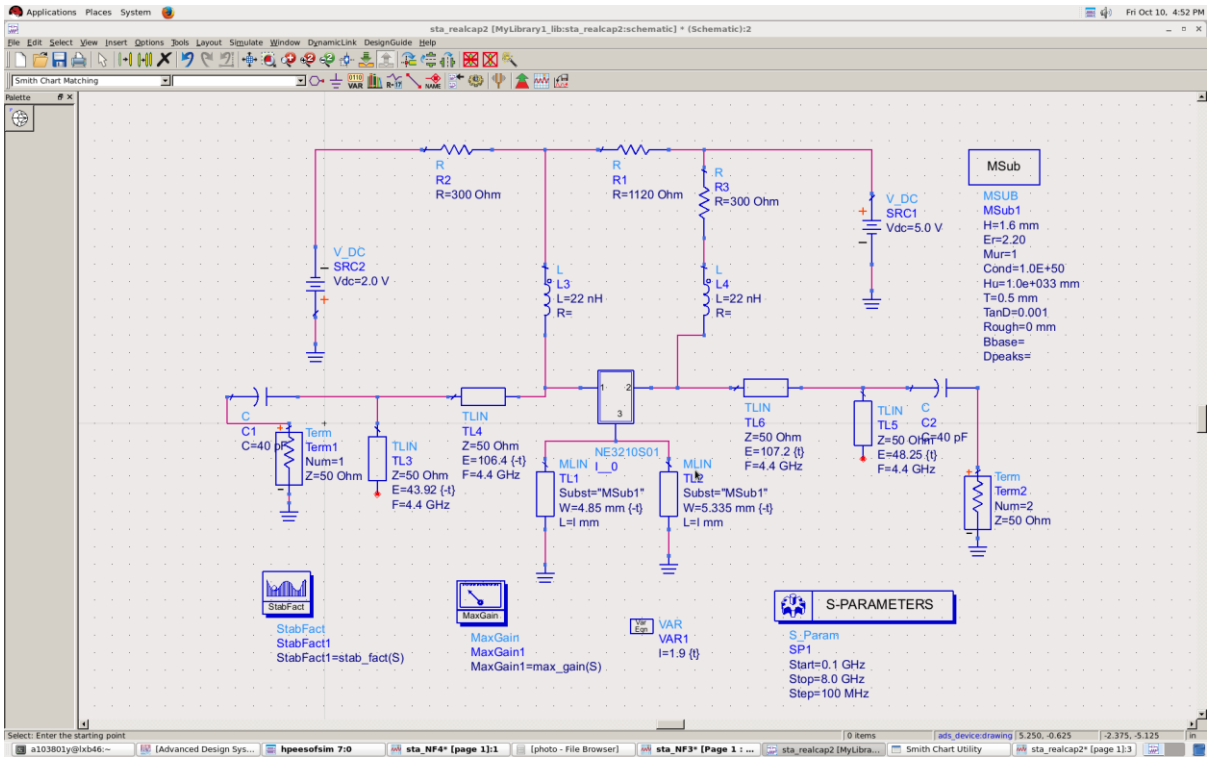


Figure (25)

Improved result is shown in below simulation (Figure 26).

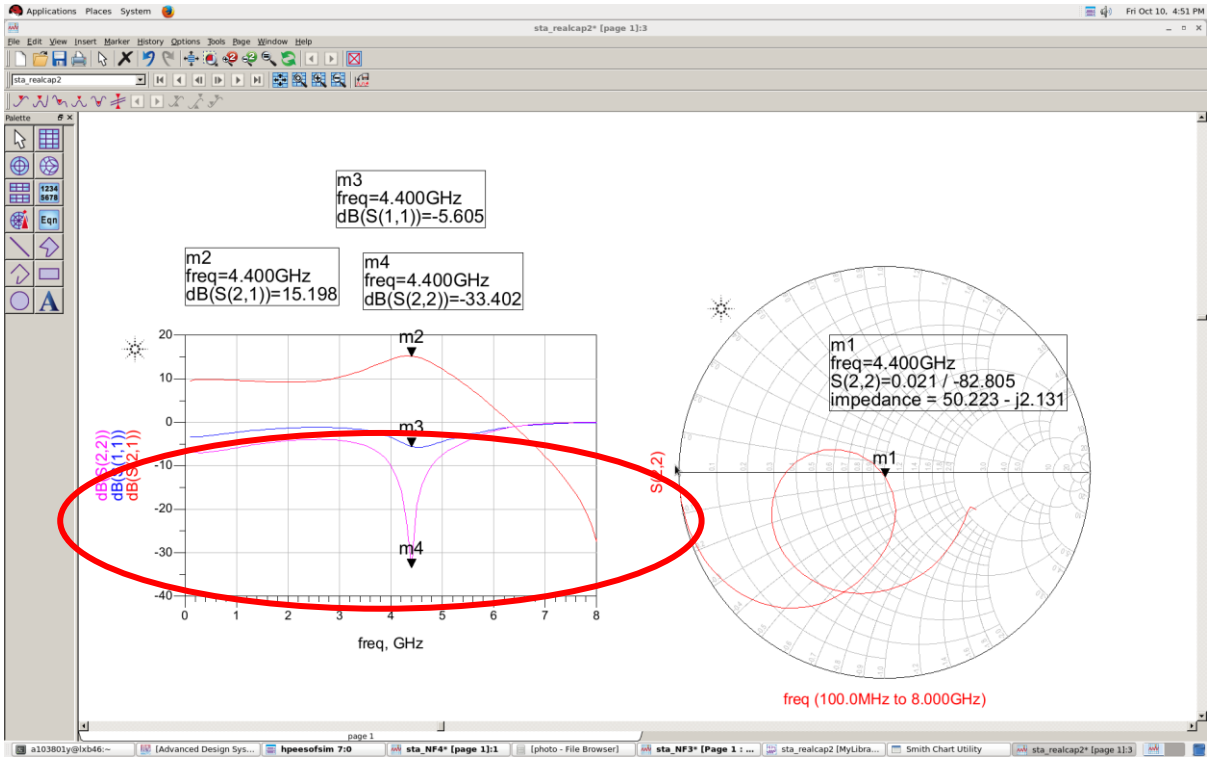


Figure (26)

It can be seen that the output return loss is very good and gain has been improved to 15.198dB.

Matching Network Implementation

In ADS, LineCalc is a very useful tool to implement the ideal matching netwroks using microstrip transmission lines. The physical length can be dtermined using the LineCalc. All microstrip lines and their electrical length are listed below.

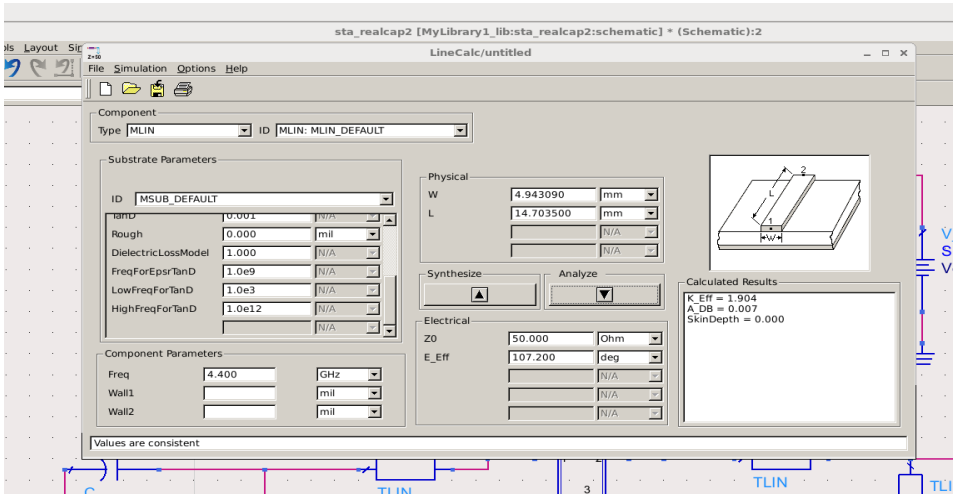


Figure (27)

Calculation the physical length value using LineCalc, can be found below table.

	Electrical length (degrees)	Physical length (mm)
TR3	43.92	6.02
TR4	106.4	14.59
TR5	48.25	6.62
TR6	107.2	14.7

Then replace all ideal transmission lines with the micro-strip lines. To improve stability and gain, the calculation value is still required to tune and refer to schematic below Figure28.

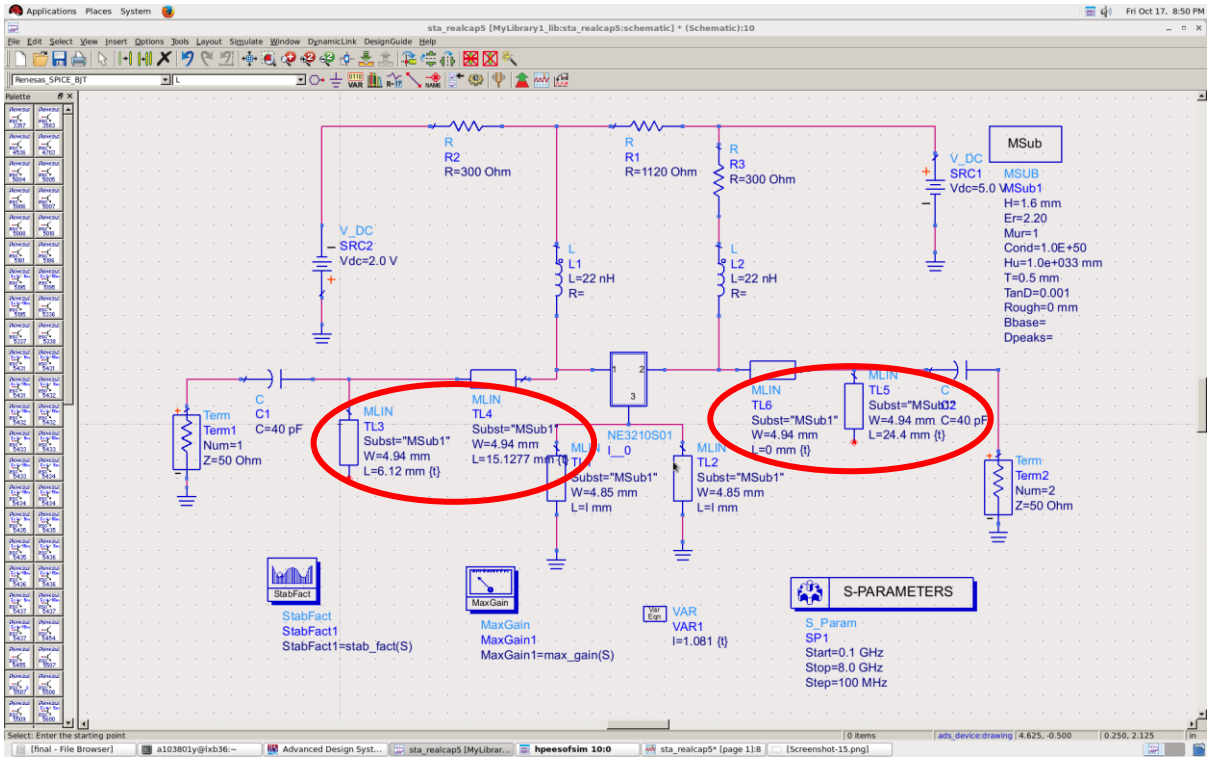


Figure (28)

Simulation result is refer to below Figure 29.

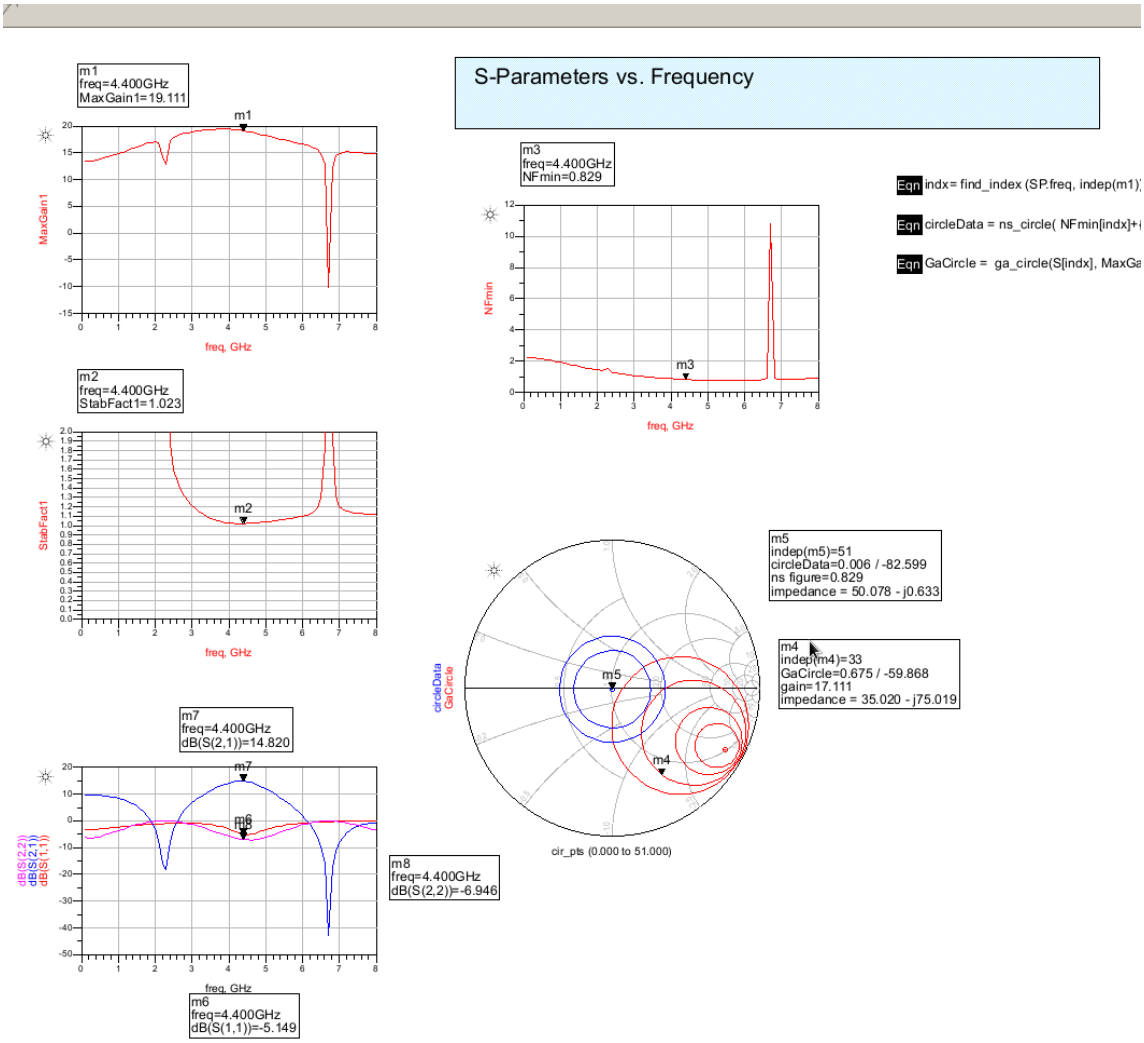
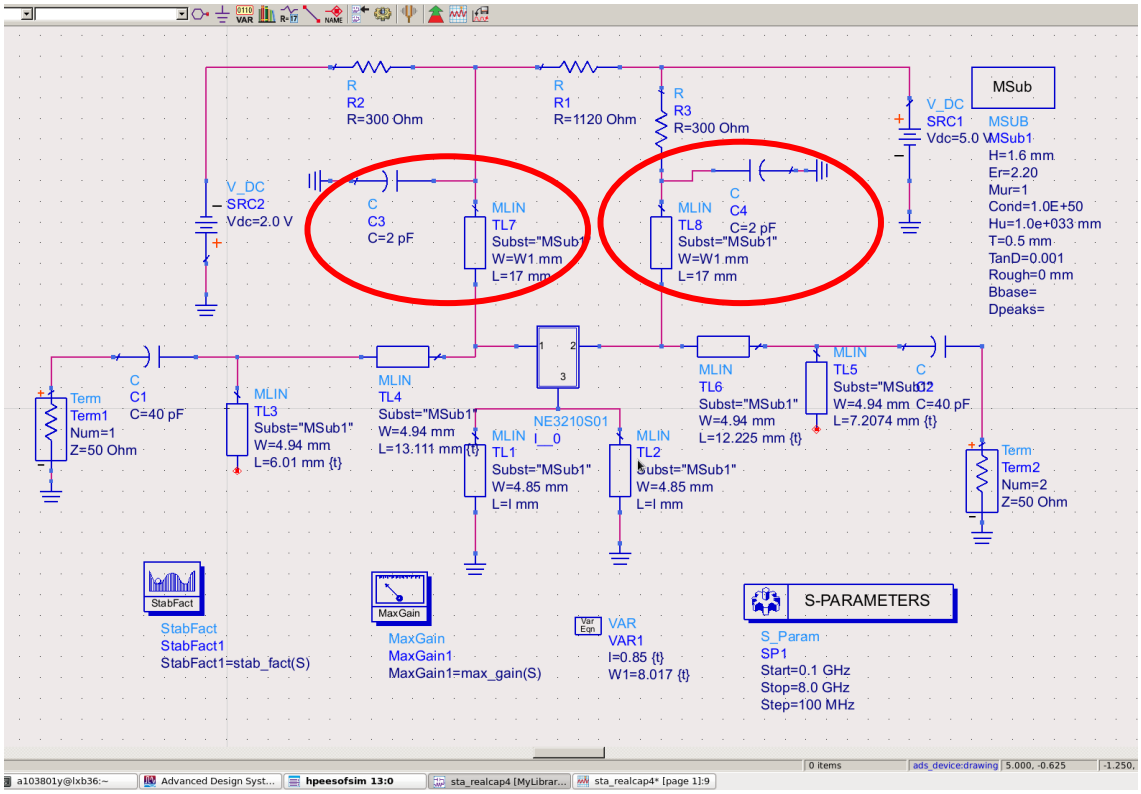


Figure (29)

Due to inductors may no perform well in the real application in the high frequency condition, replace the inductors with transmission lines of ¼ wavelength and capacitors. In order to get better performance, tuning need to be done and required to use 2pF capacitor. Final schematic is refer to below figure 30.



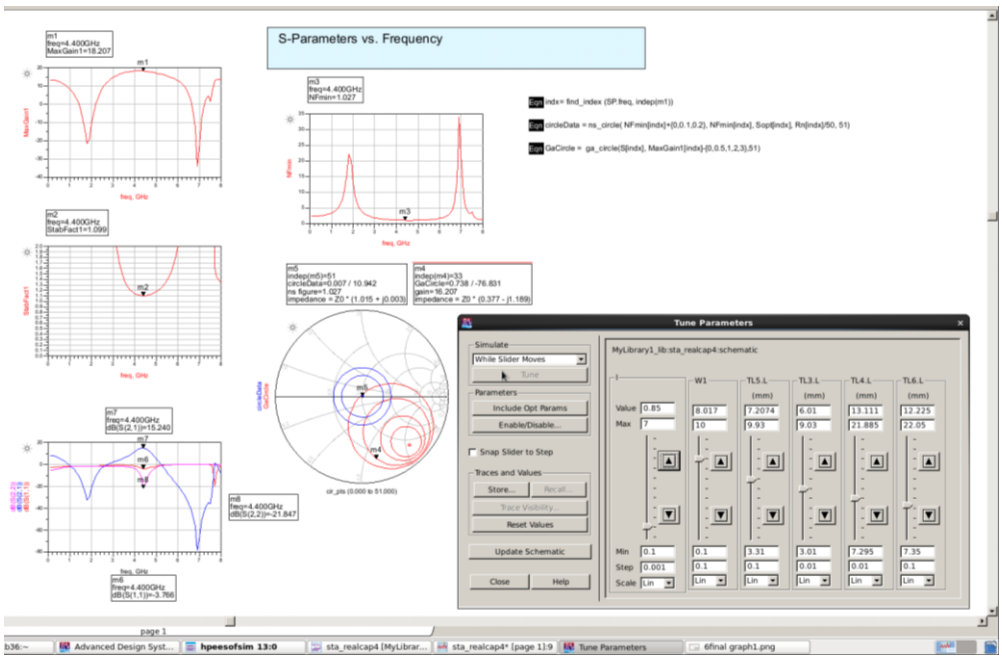


Figure (30)

Improved simulation result can be found in Figure 31.

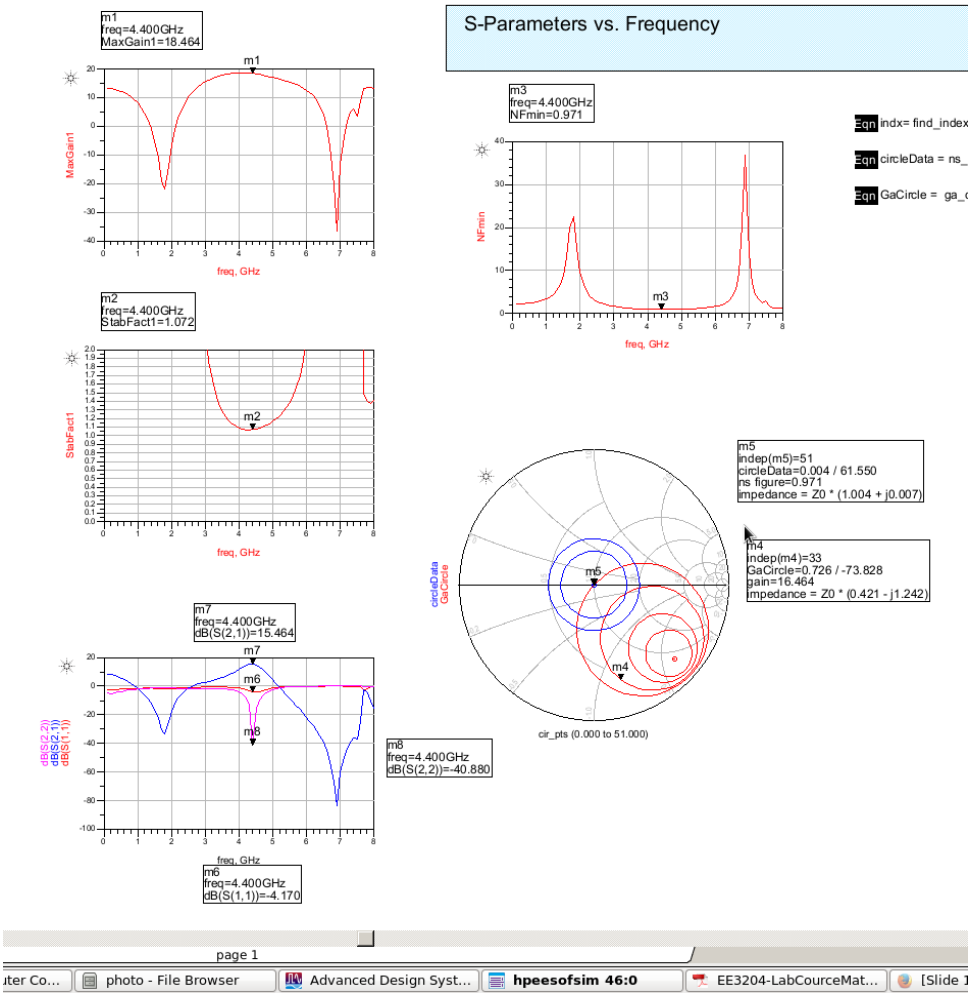


Figure (31)

Final schematic and final layout

After the initial simulation, the performances are not very ideal. Some tuning and optimization are needed to be perfect the design. After that, the schematic needs to be transferred into a layout specific schemtic. To ensure a proper layout, the following modifications should be done:

(1) Adding Tee netowrks for branching in the layout where necessary.

(2) Adding some small length of transmission line to connect the pads of devices to other transmission lines.

The final schematic after tuning the lengths of transmission line to get better performance is shown below Figure 32.

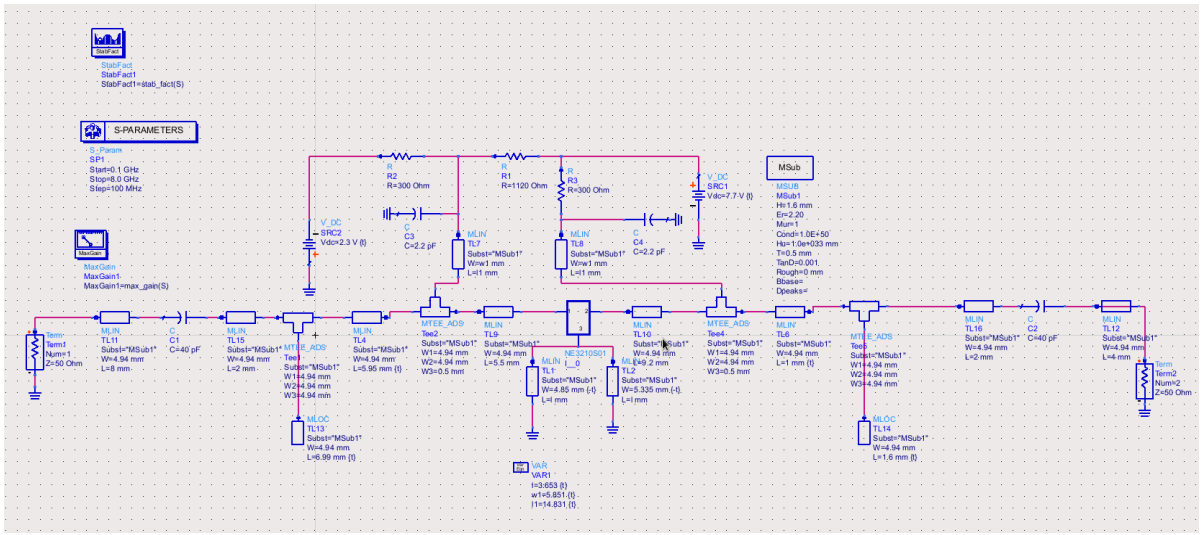


Figure (32)

Final simulation result is refer to below Figure 33.

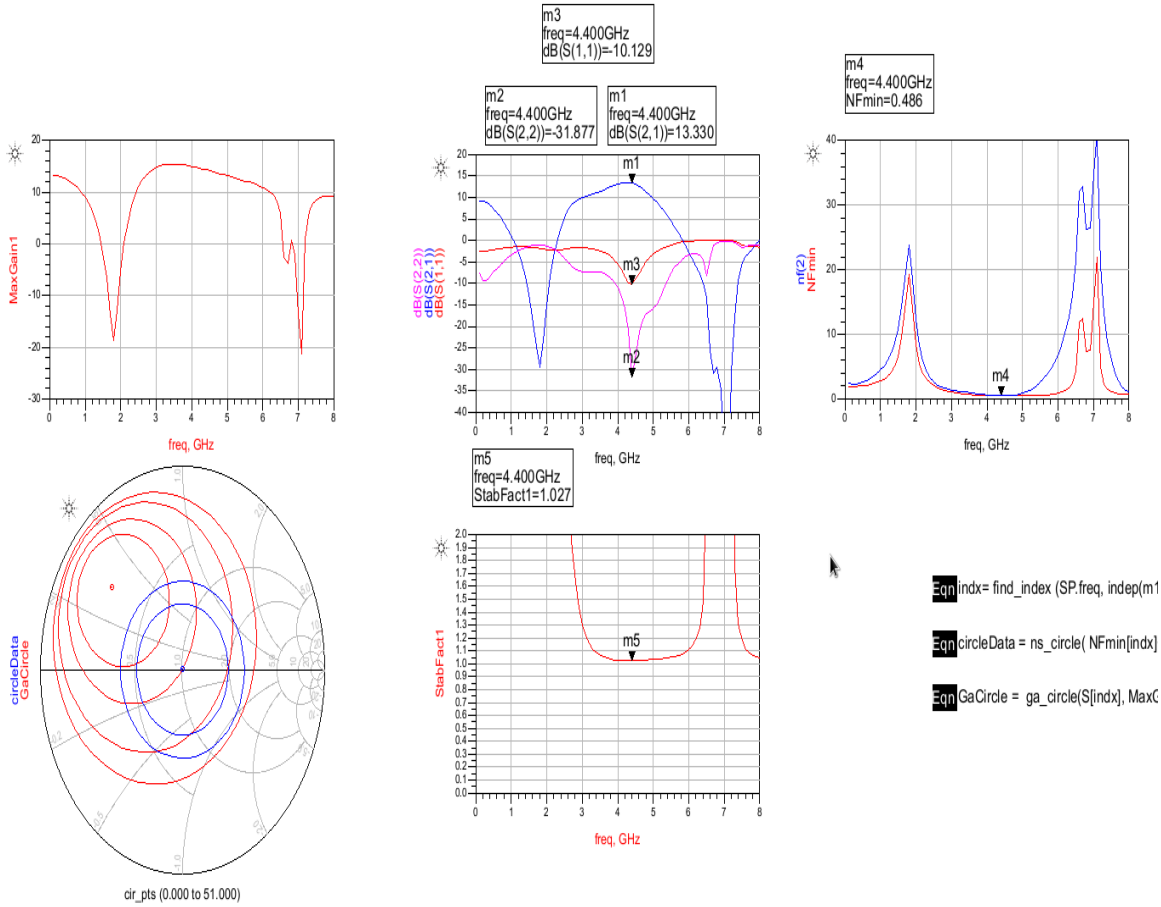


Figure (33)

CONCLUSION

From this project, team members have learned more implementation and design of a low noise amplifier using ADS software. The purpose of the amplifier is to amplify the received RF path of a Wireless local area network (WLAN). We have also gain some knowledge about the fundamental funciton of NE3210S01 which is widely in use in commercial system.

A single stage of LNA amplifier at 4.4GHz is designed in this project. This designing method enabled us to design any frequency low noise amplifier using ADS. Also familiarizing ADS is very useful in the industry which is similar to other simulation softwares.

LNA's are very important for most of the circuits, especially in Radio Communication Systems. A product with very low noise level is very important to get an efficient output in practical cases. But we also understand that software simulaiton may vary with pratical circuits due to manufactur's components and its various specs. Aso the results are entriely depends on the environmental conditions, mainly temperature, pressure, humidity etc. But it's make the job easier to use software like ADS to plan the intial circuits rather than jump into the direct designing.